TELEDYNE LECROY
Everywhereyoulook™

Kibra™ 480
DDR3 / DDR4 Protocol Analyzer

DDR3 / DDR4 BUS & TIMING ANALYSIS

Key Features

- **Fast and Easy Debug for DDR3 and DDR4**
  - **— Self-contained system offers easy connection and setup**
  - **— Custom probe design supports higher speed modules**
  - **— No calibration needed!**
  - **— Free trace viewer runs on any PC**
- **Comprehensive JEDEC Trigger and Capture**
  - **— Detects over 65 JEDEC bus event & timing violations in real time**
  - **— Extended recording time captures 4X the memory events vs. Logic Analyzer**
  - **— Interposers capture SPD data for fast configuration of the analyzer**
  - **— Dedicated trigger output to scope for Read/ Write operations**
- **Innovative Displays Focused on Timing Analysis**
  - **— Traditional State and Timing Waveform views**
  - **— Visualize I/O distribution with the Bank State View**
  - **— Bus metrics are tracked per bank and per DIMM slot**
  - **— Real Time performance displays**
- **Flexible, Scalable Platform**
  - **— Monitor two slots of quad rank DDR3 or DDR4 DIMMs concurrently**
  - **— Supports registered and unbuffered DIMM types**
  - **— Address multi-channel application by cascading analyzers**

Kibra™ 480 DDR4 Protocol Analyzer

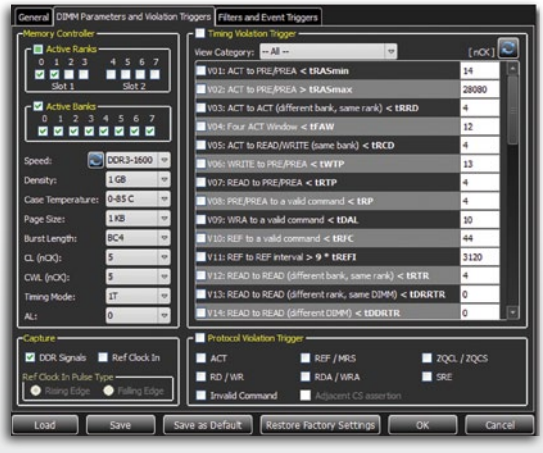
The Teledyne LeCroy Kibra™ 480 is a stand-alone protocol analyzer that provides comprehensive DDR3 and DDR4 JEDEC timing analysis. Based on the ground breaking Kibra 380, the 480 platform introduces proprietary probing technology designed to non-intrusively monitor higher speed DDR3 as well as the new DDR4 specification without time consuming calibration and setup. Sitting in-line on a live system, the analyzer records bus traffic while automatically identifying timing and protocol violations. It displays both commands and errors using a full function waveform viewer allowing fast debug of memory devices and controllers.

Proprietary Probe Design for higher speed memory

Teledyne LeCroy developed a custom ASIC for the Kibra 480 probe to support higher speed DDR modules. This proprietary probe implementation allows loss-less capture of DDR3 to 2133 MT/s; and DDR4 to 2400 MT/s. The probes are self-powered to provide instant signal lock – including reliable capture of the DDR4 power-on sequence. Separate probes are available for DDR3 and DDR4 supporting both U-DIMM/R-DIMM as well as SO-DIMM form-factors.

Easy Setup— No Calibration Needed!

Start using the Teledyne LeCroy Kibra 480 immediately without time consuming calibration. Simply enter the memory controller parameters and start recording. The software will automatically load JEDEC trigger values for the DIMM type specified. Users can selectively disable or override any of the JEDEC triggers on-the-fly.



JEDEC timing values load automatically based on memory parameters.

Accurate wave-form display of all physical address attributes (RA, CA, BA, CS)

Timing Navigation bar allows fast zoom-in

Annotate and analyze traces with custom markers

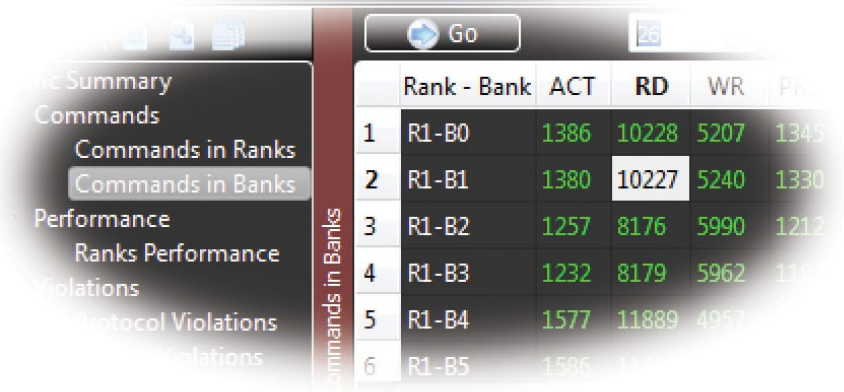
State listing shows all command information including timing errors

Visualize I/O distribution with the Bank State View

Use event metrics to navigate to individual commands, addresses or violations

Traffic Summaries for Faster Analysis

In addition to timing analysis, the Kibra 480 generates performance metrics that are displayed for read, write and power down operations. Bus metrics are tracked per bank, per rank, and per channel to provide insights into overall memory utilization. The error report shows protocol and timing violations with hyperlinks to the error in question.

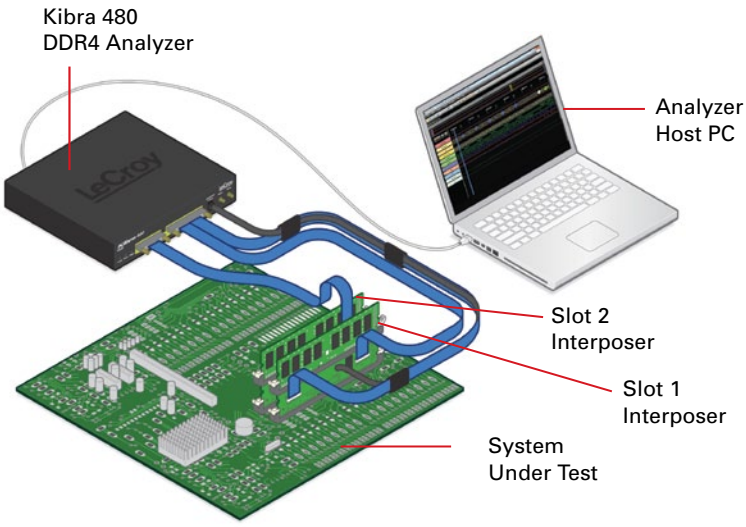


Search for commands by Rank or Bank Address.

SPECIFICATIONS AND ORDERING INFORMATION

Custom Sequential Event Triggering

The Kibra 480 can specify custom triggers for any DDR command including MRS or Read/Write commands to a specific physical address. With the sequential triggering, the analyzer can wait for any two command/control states in sequence including any combination of high/low signaling. Optionally add a timer within the sequence to specify a timeout condition or re-arm the analyzer. Filtering of NOP & Deselect commands is available to selectively capture the most important operations. There's also a low-latency trigger-out that can signal over SMA any time a read or write operation occurs. Using this real time trigger-out makes it easy to distinguish between Reads and Writes on an oscilloscope.



Specifications

Analyzer System Specifications

Host Requirements	Intel® Pentium® 4 or AMD Duron processor or greater; USB 2.0 port: 1 GB RAM (4 GB recommended; Windows® 7, Windows XP, or Windows Vista
Protocols Supported	DDR3 and DDR4
Recording Memory Size	4 GB
Data Rates Supported	DDR3 – 400 MHz - 1066 MHz DIMM clock speeds DDR4 – 800 MHz - 1200 MHz DIMM clock speeds
Probe Interface	DDR3 & DDR4 UDIMM, RDIMM, SODIMM Slot Interposers;
Front Panel LEDs	Power, Status, Trigger
Front Panel Connectors	Cable Interface to DIMM Slot 1 Interposer, Cable Interface to DIMM Slot 2 Interposer, External RefClk-IN SMA, External Read / Write Trigger Output (SMA), Interposer Probe Power Connector
Rear Panel Connectors	CrossSync Connector, USB 2.0 Connection to Host PC: Trigger IN SMA, Trigger OUT SMA
Dimensions	(W x H x D) 20 x 3.2 x 23 cm (8"W x 1.25"H x 9"D)
Weight	1.5 Kg (3.4 lbs)
Power Requirements	External 12V Power
Environmental	Operating 0 to 55 °C (32 to 131 °F), Non-operating -20 to 80 °C (-4 to 176) Humidity: 10 to 90% RH (non-condensing)

Probe Specifications

The Teledyne LeCroy Kibra 480 is available with several slot interposer probe options that provide the mechanical and electrical interface between the analyzer and the memory system-under-test. Probes are available capable of monitoring two slots of quad rank DIMMs or SO-DIMMs operating to 2400 MT/s. The probes operate non-intrusively and introduce less than 90 ps of latency to the DDR signal.
Compatible with all standard 240-pin DDR4 SDRAM DIMM's up to 2400 MT/s.
Analysis is performed on up to 4 ranks using channel 1 slot
Analysis is performed on up to 8 ranks when using both channel 1 and channel 2 slots
18" cable length between analyzer and system-under-test

CrossSync™ Support

CrossSync is the Teledyne LeCroy analyzer synchronization framework that enables time-aligned display of protocol traffic from multiple daisy-chained analyzers. By connecting the built-in sync ports on the Kibra 480, users can monitor multiple memory channels concurrently. The same interface can also be used to synchronize DDR4 operations with bus traffic from other Teledyne LeCroy analyzers including USB, PCI Express, SAS or SATA.

Ordering Information

Product Description	Product Code
Models	
Kibra 380 DDR3 Standard Analyzer Base System	DDR-T0S3-D01-X
Kibra 480 DDR3 Standard Analyzer Base System	DDR-T0S3-D02-X
Kibra 480 DDR4 Pro Analyzer Base System	DDR-T0P4-D02-X
Kibra 480 Options for DDR4	
Kibra 480 DDR4 DIMM Slot 1 Interposer Mx Probe Kit	DDR-AC08-D02-X
Kibra 480 DDR4 DIMM Slot 2 Interposer Mx Probe Kit	DDR-AC09-D02-X
Kibra 480 DDR4 Analysis Upgrade License Key	DDR-AC09-D02-A
Kibra 480 DDR4 SODIMM Non-ECC Interposer Slot 1 Probe Mx Kit	DDR-AC14-D02-X
Kibra 480 DDR4 SODIMM Non-ECC Interposer Slot 2 Probe Mx Kit	DDR-AC15-D02-X
Kibra 480 Options for DDR3	
Kibra 480 DDR3 DIMM Slot 1 Interposer Dx Probe Kit	DDR-AC10-D02-X
Kibra 480 DDR3 DIMM Slot 2 Interposer Dx Probe Kit	DDR-AC11-D02-X
Kibra 380 Options for DDR3	
Kibra 380 DDR3 DIMM Slot 1 Interposer Probe Kit	DDR-AC01-D01-X
Kibra 380 DDR3 DIMM Slot 2 Interposer Probe Kit	DDR-AC02-D01-X
Kibra 380 DDR3 SODIMM Non-ECC Interposer Slot 1 Probe Kit	DDR-AC04-D01-X
Kibra 380 DDR3 SODIMM Non-ECC Interposer Slot 2 Probe Kit	DDR-AC05-D01-X
Kibra 380 DDR3 SODIMM EEC Interposer Slot 1	DDR-AC06-D01-X
Kibra 380 DDR3 SODIMM EEC Interposer Slot 2	DDR-AC07-D01-X
Accessories	
Mounting Bracket Kit	ACC-BRKT-013-X

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