

Dynamic Measurements of Phase Lock Loop Transient Response

TECHNICAL BRIEF

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Summary

Plotting variations in measured parameters make track functions ideal for studying the dynamics of phase locked loops.

Introduction

Teledyne LeCroy oscilloscopes are ideal tools for measuring phase error in phase locked loops (PLLs). The use of timing parameters as well as the related Track functions allows the instantaneous phase error of the PLL to be plotted as a function of time.

Figure 1 is a conceptual block diagram for a PLL.

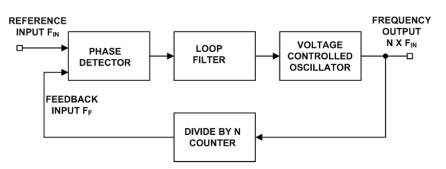


Figure 1: Conceptual Block Diagram of a Phase Locked Loop (PLL)

The phase error is the output of the phase detector. In the absence of direct access to the phase detector output, the scope can compute the phase difference between the reference and the feedback inputs. Phase difference is computed directly using the phase parameter.

The top left trace (M1) in Figure 2 is a phase modulated 66.67 MHz sinewave carrier. The phase modulation waveform is a 2 radian step function. The next lower trace (F1) is the track function of the time interval error (TIE) at the output of the PLL. The TIE function can be thought of as the instantaneous phase of the input waveform. The track function plots the instantaneous values of the measured TIE parameter as a function of time. The track function is time synchronous with the source waveform so that any variation in the track can be traced instantly to the source waveform. In this case we see the input phase to the PLL.



Figure 2: Plot of Phase error vs. time (traces F3 and Z1) for a 2 radian step phase change at the PLL input

Trace M2 is the output response of the PLL to the phase modulated input. Track F2 shows the phase response of the PLL output.

Trace F3 is the track function of the phase difference between the input (M1) and the output (M2) of the PLL. This waveform is expanded horizontally in the zoom race (Z1). This represents the instantaneous phase difference between the input and output waveforms as a function of time as a result of the 2 radian phase step in the input signal.

The phase parameter can output reading in units of radians, percent of period, or degrees. In this example we used degrees.

Parameters P4 and P5 use parameter gating to measure the mean phase before and after the phase step in the input waveform. Parameter P6 uses parameter math to compute the phase change between the input and output due to the step

Note that the output step and the jump in the phase difference begin synchronously with the input step modulation. Using the MultiZoom feature it is possible to lock the track functions with a zoom of the input waveform and then expand them all simultaneously for detailed viewing.

These same functions can be used to study how PLLs acquire lock. In Figure 3, the applied input signal (top left trace M1) is a 66.67 MHz sine carrier which is turned on at mid-screen. F1 is the track of the TIE parameter of the input. F2 is the TIE track of the output and shows the instantaneous phase of the PLL output referenced to an ideal 66.67 MHz clock.



Figure 3: A study of phase error during lock acquisition

The trace, F3, is the track function of the phase parameter and shows the phase difference between the input and output of the PLL. The zoom trace, Z1, shows the horizontally expanded view of the phase track.

Note that during acquisition the phase is changing continuously. The phase parameter measures phase modulo 180° degrees and phase values are wrapped whenever they reach \pm 180°. This continuous variation in phase is due to the frequency of the PLL output changing to 'catch up' to the phase of the reference input.

In Figure 4, the trace F4 shows a track of the parameter Frequency @ Level. This shows the instantaneous frequency of the PLL output as a function of time. This view is expanded using zoom track Z2. Z1 and Z2 share a common horizontal scale and you can see that the phase change and frequency change occur simultaneously. The absolute horizontal cursor, indicated by the cross icon, measures the final value of the frequency to be the expected 66.7 MHz.



Figure 4: A study of output frequency during lock acquisition

The use of the Jitter and Timing Analysis parameters and the associated track functions allow users to characterize the dynamic response of the PLL during lock acquisition as well as show the response to changes in the input reference signal.